EADS DEFENCE & SECURITY

APPLICATION NOTE

Understanding IEEE 1641—Signals & Triggering

An example of how signals with triggering are represented in IEEE 1641

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Introduction

This application note resulted from a query about how a particular problem involving the triggering of the waveform would be expressed using IEEE 1641.

The example in question is a fragment from a test requirement in which a sinusoid is used to trigger the application of a dc signal.

Test requirement fragment

A sinusoid signal is expected and after 3 rising edges of the sinusoid a dc voltage is to be provided. The example assumes no delay is required.

The relationship that the dc signal has to the sinusoid is that it starts immediately after 3 rising edges of the sinusoid. The trigger intent happens outside of the signal definition of the dc voltage. The timing relationship is understood to be a decision that will be accomplished at the system level. However, there is no implication of how it will be accomplished.

```xml
<TEST REQUIREMENT >
  <Capability>
    <SignalModel:Signal name="SineWaveSignal" >
      <SignalModel:Sinusoid name="SineWave" amplitude="pk 5 V"
       frequency="60 Hz"/>
    </SignalModel:Signal>
  </Capability>
  <ChildInfo>
    <ChildTR>
      <Capability>
        <SignalModel:Signal name="DCSignal" >
          <SignalModel:Constant name="DC" amplitude="2.5 V"/>
        </SignalModel:Signal>
      </Capability>
    </ChildTR>
    <TriggerIntent type="risingEdgeCountComplete" count="3"
     voltageLevel="3.5 V">
  </ChildInfo>
</TEST REQUIREMENT >
```

Possible implementations

Although the test requirement does not specify an implementation, it is reasonable to describe two different test systems that are both capable of accomplishing the requirement.

The first system has function generator (FG) with an output trigger that can put out a sinusoid and provide a rising edge trigger on a trigger port. The first system also has an arbitrary waveform generator (ARB) with an input trigger port. These can be configured so that the FG outputs a sinusoid and provides a separate trigger signal to the ARB after three rising edges of the sinusoid, so that the ARB can turn on a dc output.

The second solution includes an ARB with a trigger input and processing capable of counting edges. These can be configured so that the FG's output is provided to the trigger port of the ARB as well as its intended UUT location. In this situation, the ARB would process the sinusoid and know when the third edge occurs so that it can output its dc signal.

The requirement can be mapped to either of these system scenarios because it does not make system decisions in the description of the relationship between signals.

The problem

How can this requirement be defined in 1641 and not demand one or the other system implementation?

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The basic solution

There is fundamentally no problem in describing such a signal using IEEE 1641 as it is currently defined.

The XML version of the problem is a segment from the overall test requirement. The XML as presented is not quite complete, because there is no link between the "SineWaveSignal" waveform (that will be used to determine the trigger point) and the trigger definition. The trigger is defined to be of type "risingedgecountcomplete", but there is no definition of this except in the accompanying text.

However, taking both the XML description and the text together, it is possible to determine exactly what the test is and from that to define a solution using IEEE 1641.

<u>The SineWaveSignal</u>

```xml
<Signal name="SineWaveSignal" Out="SineWave" >
    <Sinusoid name="SineWave" amplitude="pk 5 V" frequency="60Hz" />
</Signal>
```

<u>The DCSignal</u>

```xml
<Signal name="DCSignal" Out="DC" >
    <Constant name="DC" amplitude="2.5 V" />
</Signal>
```

<u>The Trigger Intent</u>

```xml
<Signal name="TriggerIntent" Out="RisingEdgeCountComplete" >
  <Instantaneous name="TriggerLevel" nominal="inst 3.5 V" condition="GE" />
  <EventCount name="EventCounter" count="2" Gate="TriggerLevel" />
  <EventedEvent name="RisingEdgeCountComplete" In="EventCounter" />
</Signal>
```

At this point there three separate descriptions with no link between them. These can be combined to provide desired overall Test Requirement. The XML for that would look like this:

```xml
<Signal name="DCSignal" Out="DC" >
   <Sinusoid name="SineWave" amplitude="pk 5 V" frequency="60Hz" />
   <Instantaneous name="TriggerLevel" gateTime="0.1 s" nominal="inst 3.5 V"
     condition="GE" In="SineWave" />
   <EventCount name="EventCounter" count="2" In="TriggerLevel" />
   <EventedEvent name="RisingEdgeCountComplete" In="EventCounter" />
   <Constant name="DC" amplitude="2.5 V" Sync="RisingEdgeCountComplete" />
</Signal>
```

In this XML description it is possible to identify the definition of the sine wave ("SineWave"), the definition of the trigger ("RisingEdgeCountComplete") and the fact that it is related to the sine wave by the combination of "TriggerLevel" and "EventCounter"). The definition of the dc voltage may also be identified ("DC") together with the fact that it is triggered by "RisingEdgeCountComplete".

This gives the output as shown in figure 1. The green trace shows the Sinusoid BSC ("SineWave"). The yellow trace shows the Instantaneous BSC ("TriggerLevel") being activated each time that "SineWave" signal is greater than 3 V. The EventCount BSC ("EventCounter") counts three "TriggerLevel" events and then triggers the Constant BSC ("DC") via the EventedEvent BSC ("RisingEdgeCountComplete").

Although this signal description appears to fully define the problem described above, it does have one shortcoming. The trigger is not quite correct as described as it counts the number of times that the "SineWave" has been greater than 3.5 V, and does not take into account the rising edge. This can be shown by offsetting the sinusoid by 90 deg as shown in figure 2, where the trigger fires on the second rising edge.

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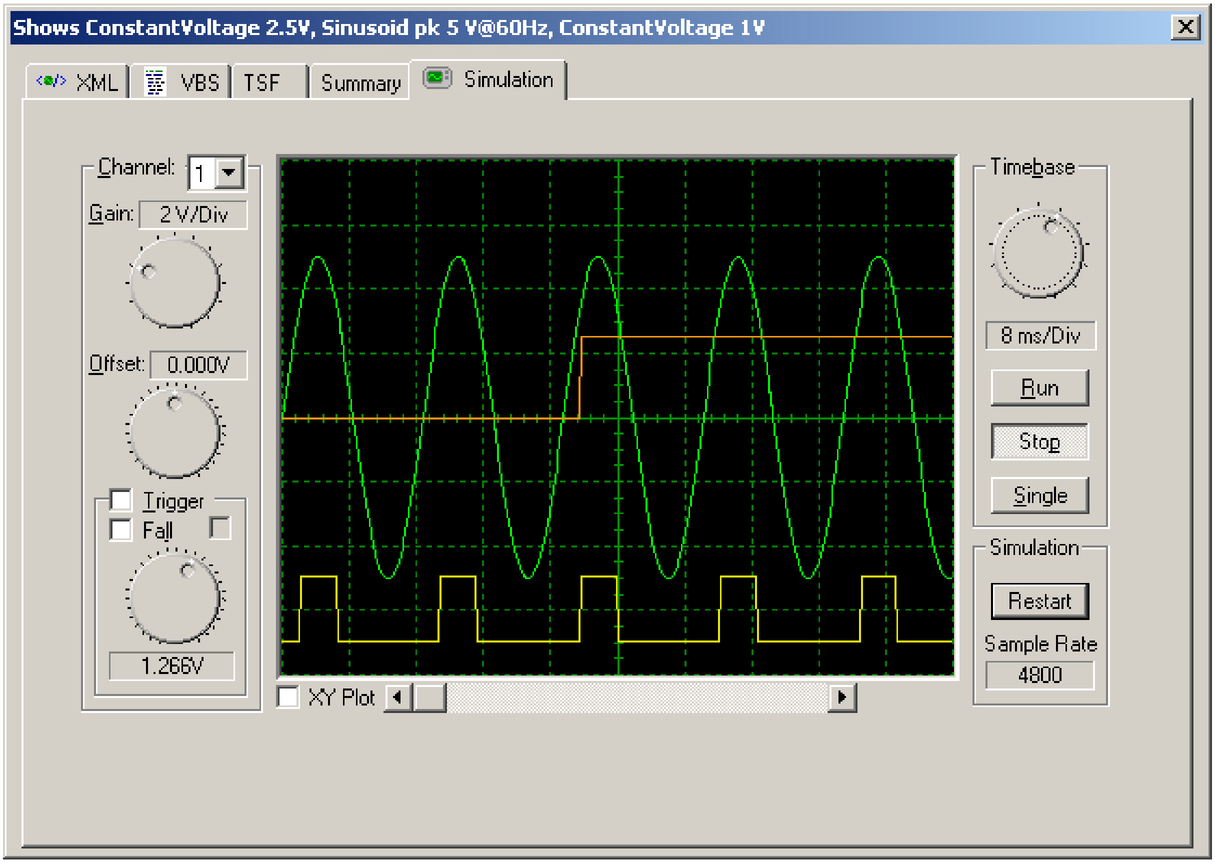

Figure 1—Output simulation showing dc voltage triggered by third cycle of sinusoid

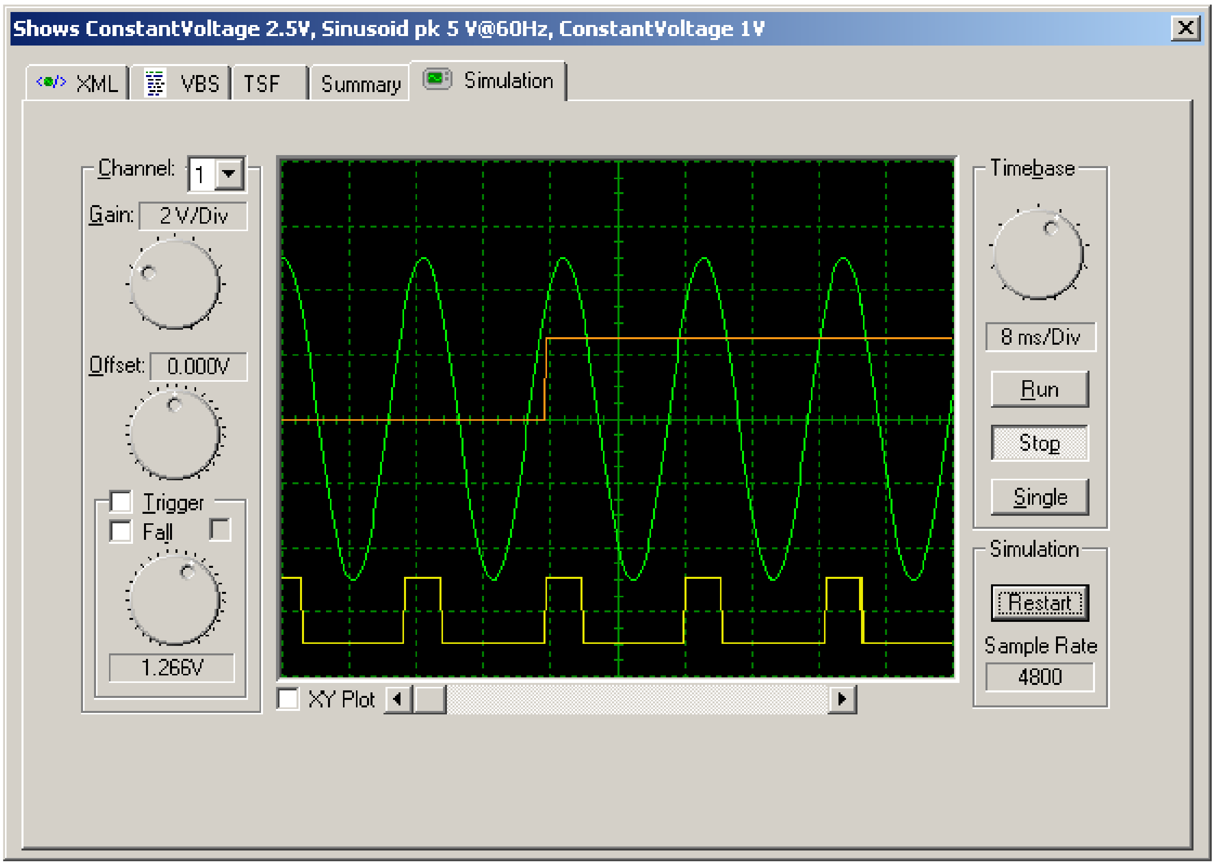

Figure 2—Output simulation with sinusoid starting with 90 deg offset

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A complete solution

The incomplete trigger information is not necessarily a point at issue, but it is good practice to get the model correct, if only to illustrate that the 1641 XML for the trigger can accurately be made to describe the trigger point related to the signal that is being assessed.

The trigger is better described as follows:

```xml
<Signal name=" TriggerIntent " Out="RisingEdgeCountComplete">
  <Instantaneous name="MustStartBelowTriggerLevel" gateTime="0.1s"
    nominal="inst 3.5 V" condition="LT" In="SineWave" />
  <Instantaneous name="TriggerLevel" gateTime="0.1 s" nominal="inst 3.5 V"
    condition="GE" Sync="MustStartBelowTriggerLevel" In="SineWave" />
  <EventCount name="EventCounter" count="2" In="TriggerLevel" />
  <EventedEvent name="RisingEdgeCountComplete" In="EventCounter" />
</Signal>
```

This ensures that the SineWave must be below 3.5 V before it starts counting events, as shown in figure 3.

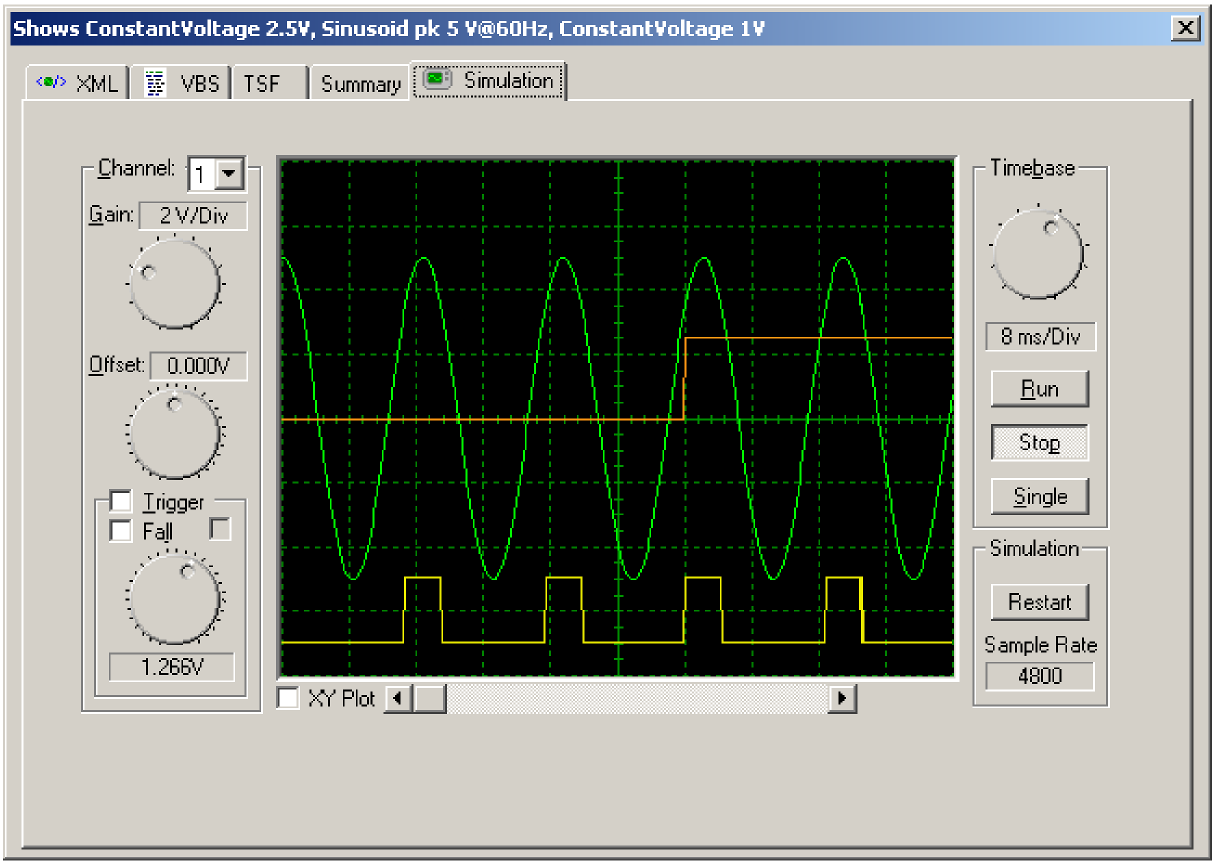

Figure 3—Simulation showing trigger on rising edge

Although this looks complicated for the trigger description, it can be described once in a TSF model and reused. It is also accurate and leaves no room for misinterpretation.

The important issue here is that this describes exactly when the trigger is required related to the sinusoid, and is correct whether the sinusoid is output by an FG, an ARB, or even the UUT. The two scenarios described in the original problem above are both possible implementations of the 1641 test description. This requires the implementer to understand the requirement (as clearly defined in 1641) and to implement the test using his knowledge of the way his particular test equipment works. The IEEE 1641 definition of the test requirement is not actually demanding any particular method of implementation.

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