Using an FPGA based system for IEEE 1641 waveform generation

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***Abstract*—As the complexity and functionality of electronic equipment increases over time, testing of modern day electronics has brought about the need for more complex stimulus and measurement capabilities. New methodologies such as Virtual and Synthetic Instrumentation have emerged to provide a more flexible ATE that can be re-configured to support a variety of technologies required by the modern day unit under test (UUT). Synthetic instruments can provide a solution to obsolescence in legacy ATEs and the flexibility required for commercial ATEs.**

A project was initiated to implement a prototype FPGA based reconfigurable Synthetic Instrument Core Framework that could directly interpret and use IEEE 1641 signals. IEEE Std 1641 provides for the accurate definition of stimulus and measurement signals, each of which are supported by a mathematical (functional) definition.

During this project, both the software and hardware were developed for the core framework, which enabled the automatic generation and synthesis of synthetic instruments required to generate or measure a selection of IEEE 1641 signal models. The results obtained using the synthetic instruments could then be validated against simulations from EADS *newWaveX*™ signal development tool.

This paper provides an overview of the project and the processes used to determine and implement an appropriate architecture for such a synthetic instrument system. It mainly focuses on the core of the system, i.e. the controller and codec subsystems. The paper concludes by discussing the suitability of an FPGA system for an IEEE 1641 compliant synthetic instrument system, comparing synthesized signals with simulated waveforms, and indicating suitable future enhancements to the system.

Keywords-ATE; ATS; IEEE 1641; test instruments; test signals; signal generation

I. INTRODUCTION

Automatic Test Equipment (ATE) mainly consists of custom or Commercial Off the Shelf (COTS) instrumentation and an ATE controller with programming language support to provide control of the ATE's measurement and stimulus capabilities. Historically, military ATEs were programmed using the ATLAS programming language, but in 2004 the IEEE approved a new test language to more accurately define the signals needed for test. IEEE Std 1641™, IEEE Standard for Signal and Test Definition [1] is a tester independent standard for test signals and measurement definition. IEEE 1641 provides a collection of objects and associated interfaces that are used to describe signal measurement and stimulus components that are instrumentation independent. The project involved the design of a FPGA based Periodic Waveform Generator System (PWGS) that is IEEE 1641 compliant and allows dynamic attribute waveform modification. The use of a FPGA was important as it provides a generic re-configurable system that could be used to support other IEEE 1641 signals. A key feature of the system is the ability to dynamically modify the signal using the waveform attributes without modification to the hardware design. Due to project timescales, a limited number of IEEE 1641 signals were implemented, but the fundamental design will allow further signals to be implemented in the future.

II. GENERATION OF IEEE 1641 PERIODIC WAVEFORMS

A. General

In IEEE 1641, attributes are associated with the generated signal and are used to define the characteristics or behavior of that signal. As an example; a 1641 sinusoid waveform has an attribute of 'frequency' and when this attribute is dynamically changed at run time the frequency of the sinusoid waveform will also change. A program written using IEEE 1641 defines precisely what is required, but does not suggest any specific method of achieving the required result. This is left to the implementer, who is free to choose the method most suited to the ATE to be used. The 1641 signal definition may be simulated to verify that the signal provided by the ATE is the correct one. The method of generating signals used by this project directly interprets the IEEE 1641 program code and does not require any intervening conversion programs.

B. Selecting the periodic waveforms

Specific bounds were defined for this project, which limited the waveform generation to certain periodic waveforms and combinations of them. The waveforms chosen included Sinusoid, Trapezoid, Ramp, Triangle, and SquareWave. These are all defined in IEEE 1641 as Basic Signal Components

(BSCs) and may be accurately simulated using software. The Signal Modeling Language (SML) defined within IEEE 1641 may be used for very accurate simulation but the process is slow and does not provide a real time output. *newWaveX*-SD, a product developed by EADS Test Engineering Services, was used as a convenient method of obtaining simulated signals. This product has been benchmarked against the formal 1641 SML definitions and the values from these simulations were used to verify the results from the FPGA based system.

C. *Signal definition and simulation*

Fig. 1 shows a waveform that is typical of those used in this project and identifies the attributes as defined in IEEE 1641.

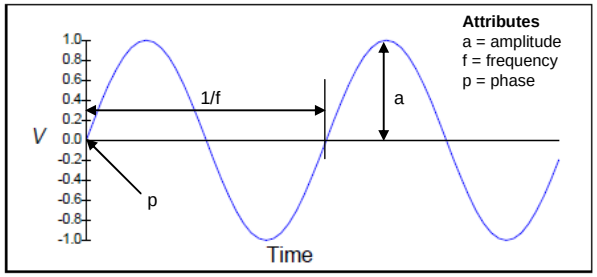

Figure 1. IEEE 1641 Sinusoid BSC with Attributes

This is a simple sinusoid, where the amplitude is given by the formula in (1).

$$a = A\sin(\omega t+\phi) \qquad (1)$$

where

A is the amplitude

ω is $2\pi \times$ frequency

ϕ is the initial phase angle

t is time

IEEE 1641 also defines combiners that perform arithmetic operations on multiple input signals to combine them into a single output. These include Sum, Product and Difference. The effect of these may also be simulated in *newWaveX*, which provides for the design and real-time simulation of test signals. Using this tool, complex signals can be modeled and simulated.

D. *Generation of physical signals*

The speed and complexity of signals that can be physically generated on hardware by *newWaveX* is dependent on the rendering device and the processor power of the PC platform. The following limitations of current rendering devices trialed with *newWaveX* are detailed in Table I.

The need has been highlighted [2] for a dedicated configurable hardware platform with dynamic signal support capability. This project focused on combiner and periodic waveform generation of 1641 signals.

TABLE I. LIMITATIONS OF CURRENT RENDERING DEVICES

Device	Limitation
PC audio card	Speed of generated signal restricted to audio frequencies
Arbitrary waveform genrators	Fixed signal requires downloading for every signal
	Very high download speed for large waveforms

A *newWaveX* model showing the combiner addition of two periodic sinusoidal waveforms is shown in Fig. 2. The *newWaveX* viewer provides a dynamic simulation of the model, as shown in Fig. 3. Modification of the waveform attributes results in an instantaneous update of the simulated waveform. The objective was to achieve the same result using hardware.

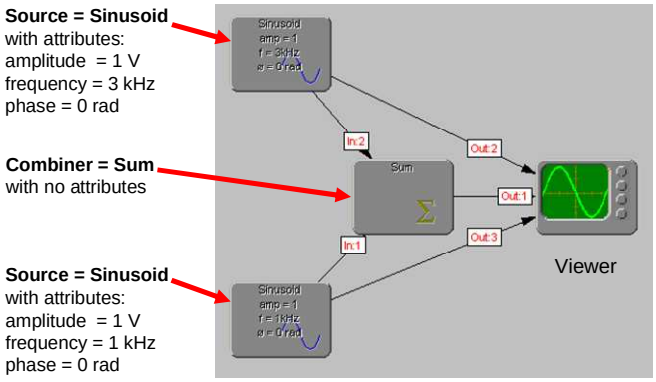

Figure 2. *newWaveX* model of combined sinusoids

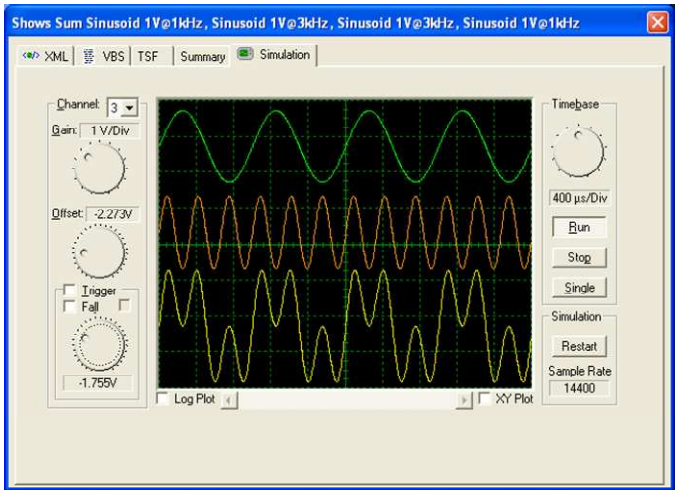

Figure 3. *newWaveX* simulation of combined sinusoids

A review of waveform generation systems was undertaken and the conclusion was that a Direct Digital Synthesizer (DDS) was the best solution for this application, especially when compared to analog methods. DDS provides fine frequency resolution over a wide range of frequencies, and is ideal use for periodic waveform generation.

Existing designs have demonstrated that DDS can be implemented in a FPGA and is easily interfaced to an embedded processor using memory mapped I/O. The inclusion of a memory lookup table in the DDS architecture provides

1641 periodic waveform generation with dynamic control of the waveform attributes. A USB communication link provides a 1641 PWGS capable of dynamic waveform generation under PC control. Following this review the architecture for a dual channel three source 1641 PWGS with combiner was defined.

III. 1641 PWGS

When combining 1641 periodic waveforms, it is important that the direct digital synthesizers are synchronized to each other to ensure the correct waveform samples are combined. The direct digital synthesizers provide a signal to allow the DDS to be stopped and re-started. The system diagram Fig. 4 shows the functional component blocks required to implement a dual channel 1641 periodic waveform generator with combiner.

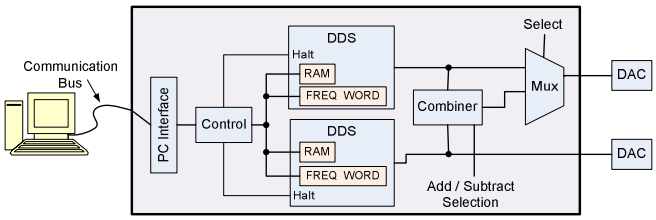

Figure 4. DDS 1641 periodic waveform generator

A. DDS Control Block

The DDS control block is required to provide the following functionality:

- Automatic generation of the 1641 discrete sample periodic waveform dependant on the attributes
- Download of the waveform lookup table (LUT)
- Control of the DDS frequency words and halt signal
- Interpretation of the PC commands.

The complexity of the control block functionality lends itself to a microprocessor based implementation. Though not based on DDS, a system architecture for an FPGA based Waveform Generator is shown in Fig. 5. This system utilizes a Xilinx MicroBlaze soft core embedded processor, Universal Asynchronous Receiver Transmitter (UART) and control logic to provide the PC communication interface and RAM update facility which is required by the 1641 Periodic Waveform generator.

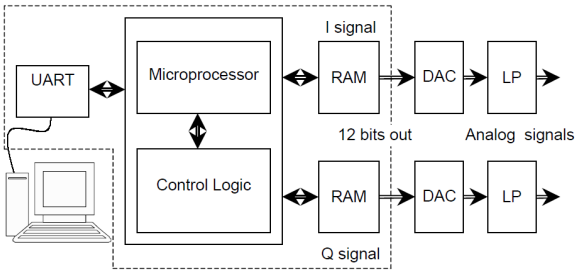

Figure 5. FPGA based waveform generator

B. Communication Bus

There is always a tradeoff between bus bandwidth and Latency in the performance of interface buses found on a modern day PC. For the transfer of large data blocks to a DDS lookup table, a data bus with a high bandwidth is required. While for multiple command transfer, a low latency bus is preferable. An ideal choice for the communication link is the PCI/PCI Express as it provides high bandwidth and low latency, and is a popular choice in commercially available waveform generators. Due to the timescales of the project it was considered a risk to design the 1641 system with a PCI/PCI Express interface, so the Universal Serial Bus 2.0 (USB) was used for the 1641 communication link as it provides a practical compromise of bandwidth versus latency.

C. PC Interface Block

The PC Interface block provides the message translation from the PC USB 2.0 bus to the control block and is dependent on the interface provided by the control block. An effective PC interface that combines both USB and UART functionality without the need for additional peripheral ICs can be realized using a JTAG UART. The Joint Test Action Group (JTAG) interface of an FPGA is used to download the design configuration to the FPGA device (Altera 2008c). FGPA vendors provide a software driver and programming cable that allow the FPGA to be configured using the PC USB port. By using the JTAG port and the JTAG UART available as IP from both Xilinx and Altera, a USB UART can be realized eliminating the need for a separate serial connection.

D. Direct Digital Synthesizer Block

1) RAM LUT: The RAM LUT of the DDS is required to accept write data from the control interface and output the phase to amplitude data to the DAC. The use of dual port RAM allows the LUT data to be updated using an independent clock at a slower rate than the higher clock rate required by the DDS to output the waveform data to the DAC. This allows the RAM LUT update to be performed at a clock rate more suited to the control block.

Another consideration when designing the RAM LUT is whether to use internal on-chip SRAM or external RAM. The use of internal FPGA SRAM eradicates the problem of speed degradation and signal integrity caused by external chip interconnection and is the principle choice for the waveform DDS LUT memory for this design.

*2) Control Block Interface:*A common peripheral interface method used in embedded systems design is memory mapped I/O. Memory mapped I/O maps the peripheral I/O device into the processor address bus memory space, allowing the processor to write directly to that device as a memory location. The use of this method requires the I/O device, in this case the 1641 periodic DDS, to implement register based control of its hardware. Fig. 6 shows the use of control registers in the Arbitrary Waveform Generator. Applying memory mapped I/O control to the DDS allows the control block to write to the LUT, update the frequency word and stop and start the DDS and is the preferred option for the design.

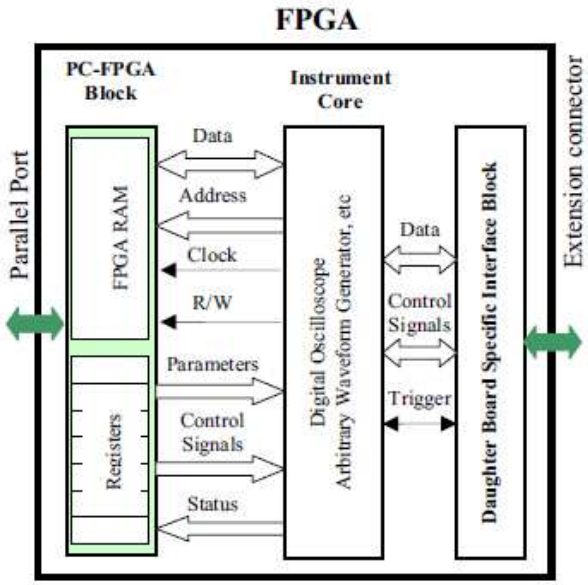

Figure 6. FPGA based instrument control using registers

E. 1641 Periodic Waveform Generator Summary

The architecture for a dual channel three source 1641 PWGS with combiner can be defined and is shown in Fig. 7.

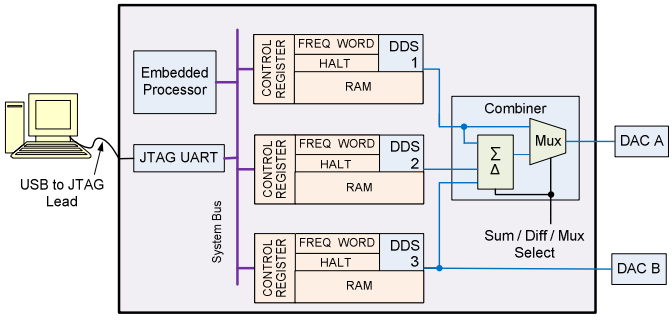

Figure 7. 1641 Periodic Waveform Generator System

IV. PRACTICAL SOLUTION

Using the system architecture detailed above and shown in Fig. 7, the 1641 PWGS was designed and synthesized into a FPGA bit stream for download into the development platform. The resultant system is summarized in Fig. 8, Fig. 9 and Fig. 10, which show the build up of the 1641 PWGS. Fig. 8 shows the numerically controlled oscillator (NCO) that was used as the basis of the 1641 DDS. It required the addition of a multiplexor to allow the wavedata register to be read by the microprocessor. The dual port RAM allows the DDS to operate at a different system clock frequency than the processor or be driven by an external clock. It was also designed so that the Halt signal could be used for synchronization of multiple DDSs.

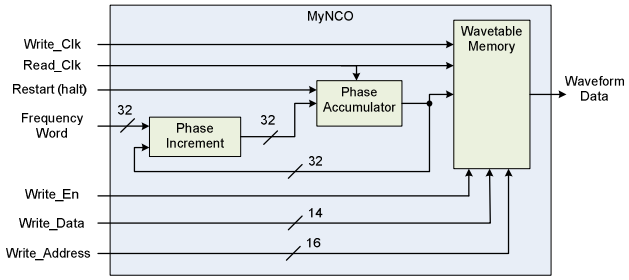

Figure 8. NCO used as part of 1641 DDS

The DDS then required further modification to convert it into a custom component (an Avalon MM Slave Component) that could be included in the System On a Programmable Chip SOPC). Fig. 9 shows the 1641 SOPC. The 1641 top level PWGS is shown in fig. 10.

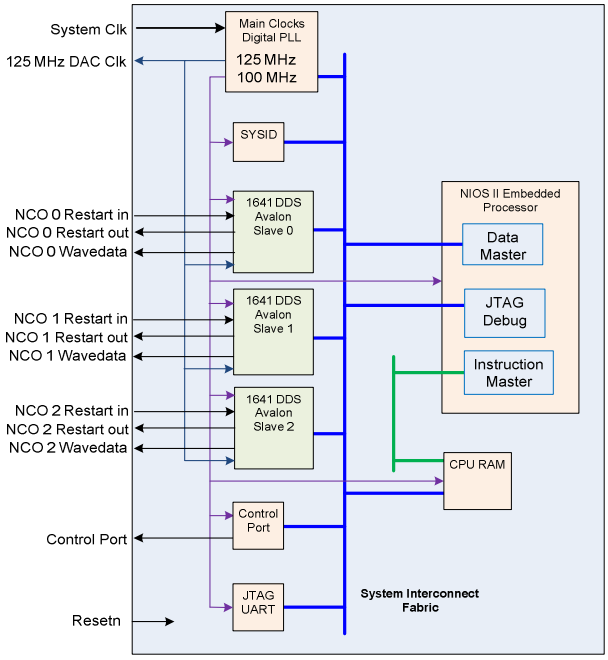

Figure 9. 1641 System On a Programmable Chip

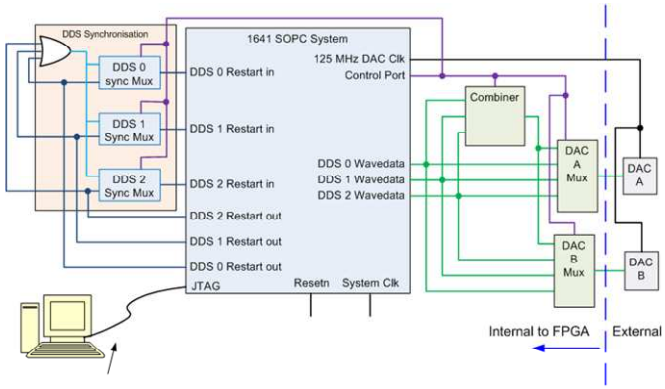

Figure 10. 1641 top level PWGS

The application software to control and exercise the systems functionality was written and commissioned and provided the test conditions that were used to verify the performance of the 1641 FPGA based periodic waveform generator system.

V. System Verification

The performance and operation of the 1641 PWGS and its constituent components shown in Fig. 10 were verified by comparison of the measured results and the simulation results. Measurement was performed using an oscilloscope, spectrum analyzer and universal counter. The Hewlett Packard 8591E Spectrum Analyzer was used to perform the frequency domain measurements on the 1641 sinusoid waveform. The RACAL-DANA 1992 universal counter was used for frequency and period measurements, while the Hewlett Packard (HP) Infinium oscilloscope was used to measure the remaining 1641 periodic waveform attributes.

Detailed measurements and comparisons of all the characteristics itemized in Table II were performed.

TABLE II. Performance Characteristics Measured & Compared

Functionality	Characteristic
1641 DDS Component Key Performance	Spurious Free Dynamic Range Verification
	Frequency Verification
1641 PWGS Functions	Spurious Free Dynamic Range
	Amplitude Attribute
	Phase Angle Attribute
	Frequency Attribute
	Period Attribute
	Rise Time Attribute
	Pulse Width Attribute
	Fall Time Attribute
	Duty Cycle Attribute
	newWaveX Simulation Comparison
1641 PWGS Combiner Functions	Summation Functionality
	Difference Functionality
	newWaveX Simulation Comparison

As an example of the measurements and comparisons performed for each element in Table II, the results for the Combiner Difference functionality checks are provided. The three square wave signals used for the difference measurement had the attributes shown in Table III.

Table IV shows the difference measurements for three square wave signals.

Fig. 11 & Fig. 12 show the comparison of the generated difference signal with the simulated difference signal.

TABLE III. SquareWave Attribute Values

	amplitude	frequency	dutyCycle
DDS 0	0.25 V	1 MHz	50%
DDS 1	0.25 V	1 MHz	30%
DDS 2	0.25 V	1 MHz	20%

TABLE IV. SquareWave Difference Measurements

Difference Amplitude Attribute	Measured Amplitude
1.000 V	0.998 V
0.925 V	0.923 V
0.850 V	0.851 V
0.775 V	0.776 V
0.700 V	0.701 V
0.625 V	0.625 V
0.550 V	0.548 V
0.475 V	0.479 V
0.400 V	0.402 V
0.325 V	0.326 V
0.250 V	0.249 V
0.175 V	0.175 V
0.100 V	0.100 V
0.025 V	0.025 V

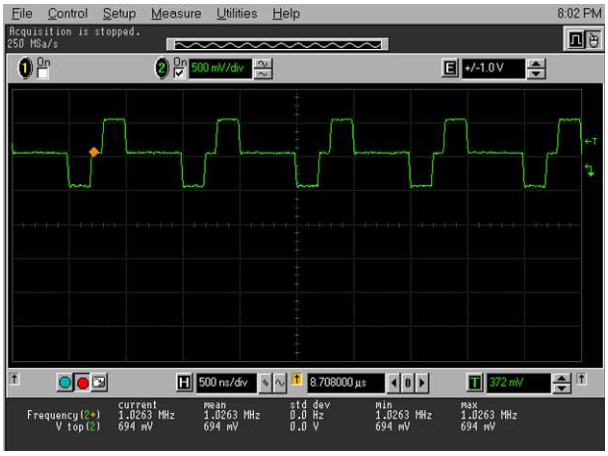

Figure 11. Waveform captured from 1641 PWGS

The verification measurements conducted on the 1641 PWGS have shown that modification of the waveform attributes produced the expected change to the waveform, as defined by the 1641 standard. They have also shown that the waveforms generated by the system are comparable to those obtained using the *newWaveX* simulator. A detailed analysis of these results was conducted to ascertain the accuracy and performance of the 1641 PWGS and to provide a comparison of performance against a commercial function generator.

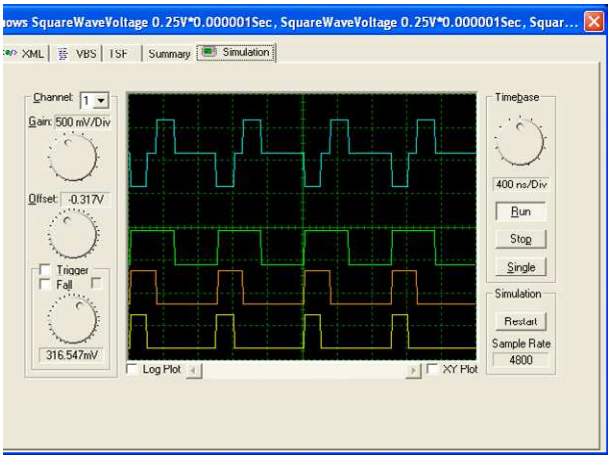

Figure 12. Waveform simulated by *newWaveX*

VI. Analysis of Results

Initial verification was focused on the performance of the 1641 DDS, with the results being compared to the Altera DDS. The Spurious Free Dynamic Range (SFDR) measurement was conducted to determine the spectral purity of the 1641 DDS relative to the Altera DDS. The level and frequency of the spurs produced by the 1641 DDS were identical to those obtained with the Altera NCO, indicating the spectral purity of the 1641 DDS design was equivalent to the Altera DDS. Frequency measurements were taken with the 1641 DDS producing comparable frequency accuracies to the Altera DDS.

A. *1641 PWGS SFDR and Frequency Verification*

The SFDR and frequency measurements were repeated on the 1641 PWGS with the results compared against those obtained using a commercial function generator (Fluke PM5138A). The SFDR of the 1641 PWGS was in excess to those obtained with the PM5138A, but the spectral purity of the 1641 PWGS showed periodic spurs which were not present on the PM5138A. Further research into DDS spur reduction techniques is required to improve the spectral purity of the 1641 PWGS. Analysis of the 1641 PWGS frequency results showed that the PM5138A provided a higher resolution and frequency accuracy to the 1641 PWGS although in the range from 3 MHz to 10 kHz the 1641 PWGS obtained a notable frequency accuracy of ≈ 0.0005%. By increasing the number of bits of the DDS phase accumulator, the resolution of the 1641 PWGS could be improved to achieve the 0.1 mHz resolution of the PM51381A.

B. *1641 PWGS Attribute Verification*

The ability of the 1641 PWGS to generate compliant 1641 waveforms was assessed using the waveform test functions developed earlier to exercise and profile the operation of the 1641 PWGS. Analysis of these results showed the 1641 PWGS obtained an attribute accuracy of within ≈ 0.633% of its set value for each periodic waveform. Additional comparisons were performed using *newWaveX* to verify that the correct waveform shape was produced. The 1641 PWGS waveform generation was identical to the waveforms generated the *newWaveX* simulator.

C. *1641 PWGS Combiner Verification*

The 1641 PWGS combiner operation were assessed using the combiner test functions developed earlier to exercise and profile the combiner functionality. Analysis of these results showed the 1641 PWGS combiner obtained a measured accuracy of within ≈ 0.9% of its expected amplitude value. When compared to the amplitude accuracy of ≈ 0.633% obtained using a single periodic waveform, the combiner function was deemed to operate correctly. Additional comparisons were performed to ascertain that the correct combined 1641 Periodic waveform shape was produced using a combination of periodic waveforms and attribute settings. The 1641 PWGS waveform generator produced comparable results to the waveforms generated by the *newWaveX* simulator.

VII. Conclusions

This project and analysis of the 1641 PWGS system shows that a FPGA based system, when used in conjunction with an appropriate DAC, provides a suitable platform for the generation of the periodic waveforms defined by the 1641 standard. Research into frequency synthesis techniques highlighted a frequency synthesis methodology and system architecture that has been successfully designed and implemented on an FPGA development platform. The development platform provided all the features required by the 1641 PWGS allowing three 1641 DDSs to be incorporated into the design.

The results analysis and functional verification conducted on the 1641 PWGS have shown that the system performance is comparable to that obtained using a commercial function generator providing a practicable level of accuracy. It is anticipated that the spectral purity and frequency accuracy of the 1641 system can be improved by the implementation of DDS spur reduction techniques and increase in the number of bits of the phase accumulator.

The inclusion of the embedded processor in the 1641 PWGS allows the system to be controlled externally by a PC. This provided dynamic modification of the periodic waveform signal, using the waveform attributes in real time, in the same manner as the *newWaveX* software simulator.

The hardware design architecture provides the capabilities to incorporate further functionality into the existing 1641 PWGS system, including generation of 1641 WaveformStep & WaveformRamp signals and an arithmetic product combiner. With the periodic waveform generation of the 1641 standard successfully implemented, the 1641 system can be further enhanced to provide support for other areas of the 1641 standard, such as generation of non periodic waveforms and measurement functions.

References

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